

**Overview:**

The Viterbi Decoder IP core implements the Viterbi algorithm for decoding a bitstream encoded by a corresponding Forward Error Correction convolutional encoding system. A lot of digital communication systems incorporate a Viterbi decoder for decoding convolutionally encoded data. By using the minimum likelihood algorithm, the Viterbi decoder core is able to correct errors in received data caused by channel noise. The decoded output data is equivalent to the transmitted digital data stream.

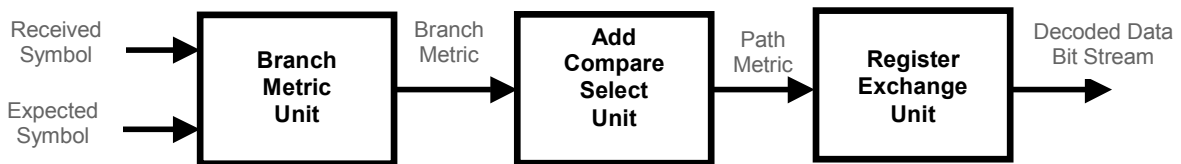
**Features:**

- Industry standard constraint length 7, rate =  $\frac{1}{2}$ , (G0, G1) = (171, 133)
- High output data rates of up to 45 Mbps
- Low latency of 111 clocks.
- Parallel architecture design
- Trace-back logic for continuous decoding
- Trace back length of 35
- Soft decision decoding
- Fully synchronous design

**Key Benefits:**

- Small silicon footprint
- High throughput/data rates
- FPGA proven on Xilinx Virtex device target.
- Bit equivalent Matlab Model available
- Elaborate Test bench.
- Customizable HDL core design
- RTL source code available for easy integration and implementation.

**Block diagram:**



**Applications:**

- Satellite communications
- Data storage devices
- Decoding Trellis-Coded Modulation (TCM) systems (telephone line modems, amateur radio, radio relay and satellite communications)

**Application Note – OFDM Receiver System:**

The OFDM receiver system performs table look-ups and MAC intensive transform operations. The system supports variable data size (4 to 16 bits) and variable data rate (40 to 320 Mbps). Data are represented as real and complex values. The system supports 8-bit precision for input and output. The FIR unit is a 127-tap FIR filter with real coefficients and the FFT unit is a 256-point complex FFT. The Slicer block is a QAM-256 demapper. The final stage is the Viterbi Soft decision decoder.



**Deliverables:**

- Core options
  - RTL design in VHDL
  - Technology specific netlist
- Bit equivalent Matlab model
- Test bench
- Documentation

**Support and warranty:**

The core is code tested, extensively simulated and thoroughly verified on hardware board. The core is warranted against defects and meets the technical specifications. In rarest case, if the core has some defects or do not comply with the specifications laid down, same will be rectified within a shortest possible time. Thirty (30) days of free technical support through telephone/e-mail/chat (voice and non-voice) is included. Additional maintenance support options available on request.

**Customization:**

Best efforts have been made to ensure that the core has most relevant features and can fit into wide range of applications. However, the customer may require some specific functions in the core. The core can be customized or modified on customers request to meet their requirement specifications.

**Target Technologies:**

- **FPGA:** Spartan 3, Virtex, Virtex 2/Pro, Virtex 4, Virtex 5
- ASIC standard cell

**Device utilization summary:**

Target Device	Max. Frequency (in MHz)	No. of slices used (out of 6912)	No. of Block RAMs used (out of 24)
Xilinx Virtex XCV600	26	1991	5



**VXL Technologies Ltd.**

No. 9/1, 14<sup>th</sup> Floor, Birla Building, R.N.Mukherjee Road, Kolkata 700 001, India  
 Tel.: +91 33 2213 3685 Fax: +91 33 2213 3686  
 E-Mail: [sales@vxldesign.com](mailto:sales@vxldesign.com) Website: [www.vxldesign.com](http://www.vxldesign.com)