

**Overview:**

The customizable Reed-Solomon IP core is optimized in terms of speed and area. The core is available for three configurations including (255, 239) and can be modified to support other configurations with symbol widths from 3 to 16 bits. The core is developed in compliance with OTN G.709 standard, but can be modified to support many different Reed-Solomon coding standards like ATSC, DVB and CCSDS. The number of symbol errors corrected can also be customized. The core is available for Xilinx Virtex-4 FPGA device. ASIC standard cell libraries flow can also be provided on demand.

**Features:**

- Supported configurations: (255, 239), (255, 223) and (511, 489)
- OTN G.709 compliant implementation.
- Symbol width: 8 and 9 bits.
- Synchronous single clocked pipeline design
- Continuous data flow operation.
- No gaps between code blocks
- Supports shortened codes.
- Detection of error symbols (when more than  $(n-k)/2$ ).
- Count of corrected error symbols (when less than or equal to  $(n-k)/2$ ).

**Key Benefits:**

- Small silicon footprint
- High speed capabilities
- Easily modifiable to implement different Reed-Solomon coding standards, symbol widths and number of symbol errors corrected.
- FPGA proven for Xilinx Virtex-4 FPGA.
- ASIC standard flow also supported according to customer needs.
- RTL source code available for easy integration and implementation

**Block Diagram:**

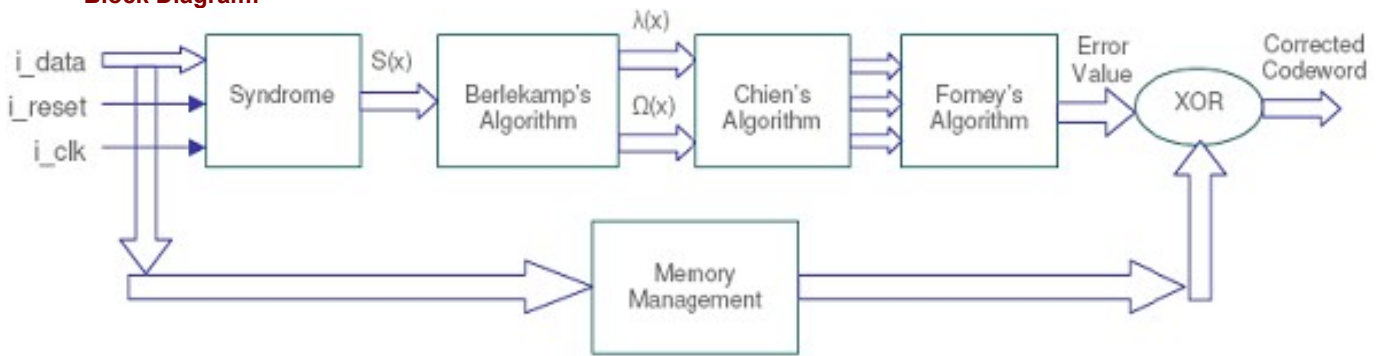


Figure 1: Decoder block diagram

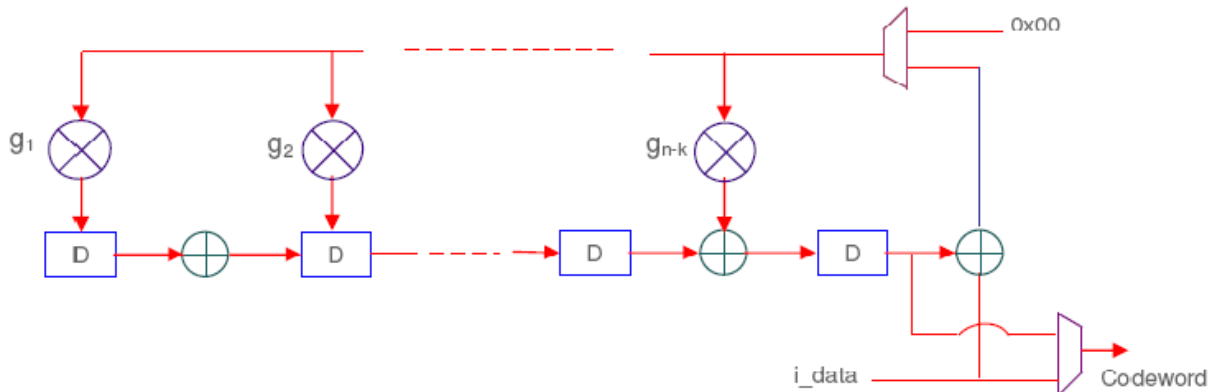
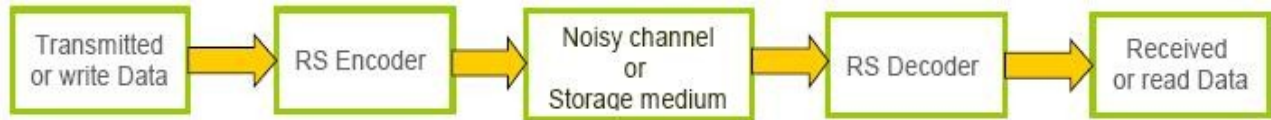


Figure 2: Encoder block diagram

### Applications:

- Forward Error Correction (FEC) codes
- Data Storage Systems
- Server Layer fo SDH, ATM, IP, Ethernet
- High speed fiber optic signals.
- Data storage systems (CD, DVD codecs)
- Data transmission like DSL systems.
- Satellite communications



### Deliverables:

- Core options
  - RTL design in VHDL
  - Technology specific netlist
- Test bench
- Documentation

### Support and warranty:

The core is code tested, extensively simulated and thoroughly verified on hardware board. The core is warranted against defects and meets the technical specifications. In rarest case, if the core has some defects or do not comply with the specifications laid down, same will be rectified within a shortest possible time. Thirty (30) days of free technical support through telephone/e-mail/chat (voice and non-voice) is included. Additional maintenance support options available on request.

### Customization:

Best efforts have been made to ensure that the core has most relevant features and can fit into wide range of applications. However, the customer may require some specific functions in the core. The core can be customized or modified on customers request to meet their requirement specifications.

### Target Technologies:

- **FPGA:** Spartan 3, Virtex, Virtex 2/Pro, Virtex 4, Virtex 5
- ASIC standard cell

### Device utilization summary:

Target Device: Xilinx Virtex xc4vsx35-12-ff668				
Core	Max. frequency (in MHz)	No. of slices used (out of 15360)	No. of RAMB16s (out of 192 RAMB16s/FIFO16)	Latency (in clock cycles)
Encoder (255, 239)	340.965	136	-	-
Decoder (255, 239)	174.375	2486	4	289
(255, 223)	158.539	3908	2	313
(511, 489)	167.108	3872	4	554



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