

Overview:

The JPEG 2000 IP core is a JPEG 2000 standard compliant encoder. The JPEG 2000 operates on a single clock domain and it can be easily integrated into any multimedia system. A synchronous Reset signal is also provided. The core is efficiently designed, synthesized for Xilinx Virtex-5 target and thoroughly verified. The JPEG 2000 IP core is available in VHDL RTL source code.

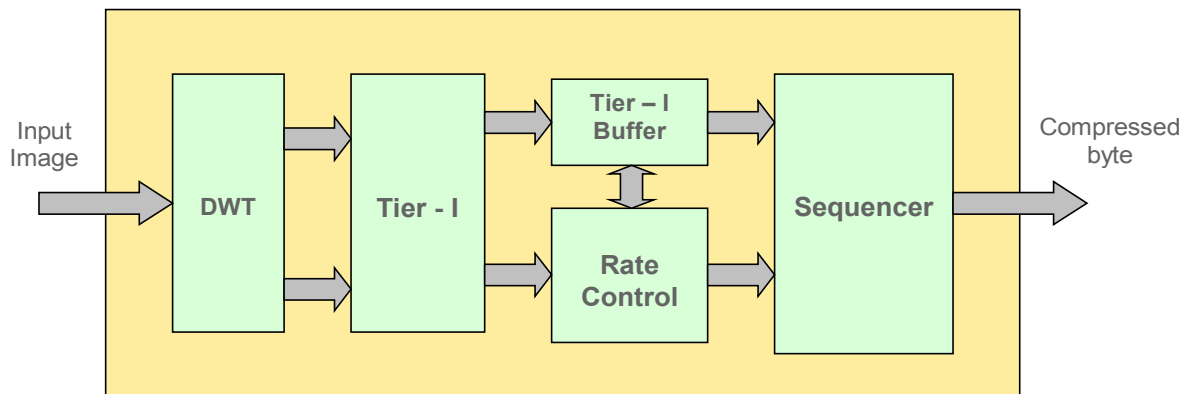
Features:

- JPEG2000 standard compliant
- User selectable lossless and lossy compression
- Rate Control
- Programmable bit rate up to 12 bits per sample
- Programmable image/tile size up to 8192 x 512
- JPEG2000 graphics file format (.j2k) output
- Large Frames Processing without unpleasant Blocking Artifacts
- Fairly brisk input pixel rate in excess of 75 MSamples/Sec
- Fully synchronous single clock design.
- Internal Memory System architecture

Key Benefits:

- Low target device memory and logic silicon footprint
- Motion JPEG support available (optional)
- Bit equivalent C model provided
- Customizable HDL design.
- Easily modifiable design to meet specific requirements
- FPGA proven for Xilinx Virtex-5 FPGA.
- RTL source code available for easy integration and implementation

Block diagram:

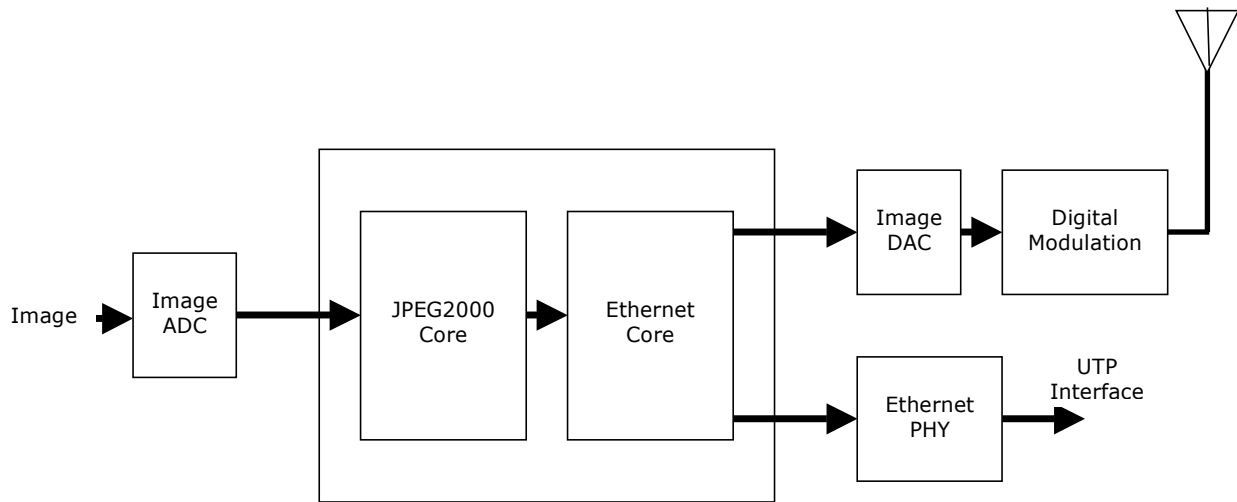


Applications:

- Consumer Electronics (Digital Cameras, Mobile Phones, Printers, Scanners)
- Client/Server communication (Internet, Image database, Video Streaming)
- Military, Digital CCTV and surveillance systems (HD Satellite Images, Motion detection)
- Medical Imagery
- Remote Sensing
- High Quality Frame based Image/Video recording, editing and storage systems.

Application Case Study – Digital Image Distribution:

This application implements an intelligent image transport system for the Video Surveillance, Defence, Space and Telecom industry. It involves compression of the input image stream using the JPEG 2000 IP core and transmission of the compressed image over Ethernet or a digitally modulated wireless protocol.



Deliverables:

- Core options
 - RTL design in VHDL
 - Technology specific netlist
- Bit equivalent C model
- Test bench
- Documentation

Support and warranty:

The core is code tested, extensively simulated and thoroughly verified on hardware board. The core is warranted against defects and meets the technical specifications. In rarest case, if the core has some defects or do not comply with the specifications laid down, same will be rectified within a shortest possible time. Thirty (30) days of free technical support through telephone/e-mail/chat (voice and non-voice) is included. Additional maintenance support options available on request.

Customization:

Best efforts have been made to ensure that the core has most relevant features and can fit into wide range of applications. However, the customer may require some specific functions in the core. The core can be customized or modified on customers request to meet their requirement specifications.

Target Technologies:

- **FPGA:** Virtex 4, Virtex 5
- ASIC standard cell

Device utilization summary **:

Target Device	Max. Frequency (in MHz)	Slices used (out of 51840)	Block RAMs used (out of 288 Block RAM / FIFO)
Xilinx Virtex xc5v1x330ff1760	111	23274	262

** 10 bits per pixel; 5/3 DWT type



VXL Technologies Ltd.
 No. 9/1, 14th Floor, Birla Building, R.N.Mukherjee Road, Kolkata 700 001, India
 Tel.: +91 33 2213 3685 Fax: +91 33 2213 3686
 E-Mail: sales@vxldesign.com Website: www.vxldesign.com