

Overview:

The Ethernet IP core is a IEEE 802.3-802.3u compliant 10/100 Ethernet Media Access Controller (MAC). An external PHY can be connected for a complete Ethernet solution. This core is On-Chip Peripheral Bus (OPB) v2.0 compliant. A flexible implementation makes this IP core suitable for all kind of Ethernet applications. The Ethernet IP core is available in Synthesizable mixed VHDL-Verilog RTL code.

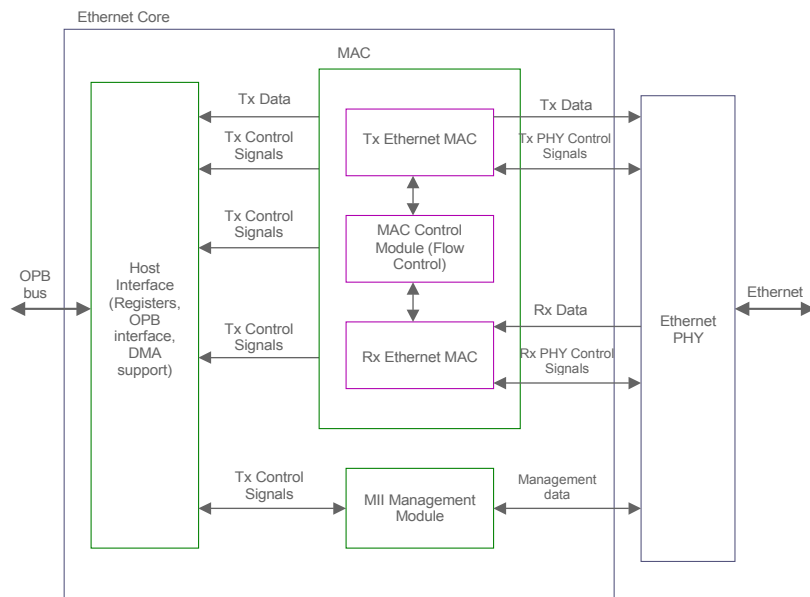
Features:

- Performing MAC layer functions of IEEE 802.3
- Automatic 32-bit CRC generation and checking,
- Delayed CRC generation
- Preamble generation and removal
- Automatic padding of transmitted short frames
- Detection of excessive long or excessive short packets
- Optional transmission of packets bigger than standard size
- Full duplex operation
- 10 and 100 Mbps bit rates
- 32-bit System Data Bus interface
- Automatic packet abortion on excessive deferral limit or too small inter packet gap
- Flow control and automatic generation of control frames in full duplex mode (IEEE 802.3x)
- Collision detection and auto retransmission on collisions in half duplex mode (CSMA/CD protocol)
- Complete status for TX/RX packets
- IEEE 802.3 Media Independent Interface (MII)
- On-Chip peripheral bus (OPB) v2.0 compliant interface
- Internal RAM for holding 128 TX/RX buffer descriptors
- Interrupt generation on all events

Key Benefits:

- Targeted for low-cost Xilinx Spartan-3 series FPGA
- OPB bus interface
- Customizable, highly configurable and modular core design
- Minimum resource usage
- High throughput capabilities
- RTL source code available for easy integration and implementation

Block diagram:

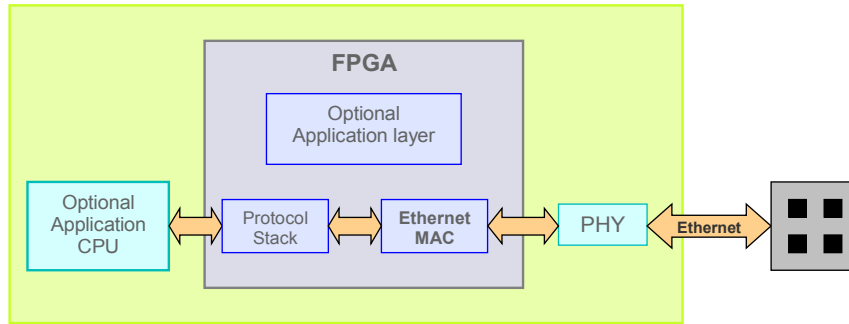


Applications:

- Ethernet based servers and network attached storage devices
- Storage Interconnects
- Network based Video-on Demand
- Wireless Ethernet data communication equipments (wireless Ethernet radio modems)
- Wide area, Storage area, Local area, Metro area networks

Application Note – Industrial Ethernet System:

Figure shows an Ethernet MAC IP core based Industrial Ethernet system. The IP core resides in an FPGA, which when combined with an Ethernet transceiver (PHY) can perform all Ethernet protocol functions.



Deliverables:

- Core options
 - RTL design in mixed Verilog, VHDL
 - Technology specific netlist
- Test bench
- Documentation

Support and warranty:

The core is code tested, extensively simulated and thoroughly verified on hardware board. The core is warranted against defects and meets the technical specifications. In rarest case, if the core has some defects or do not comply with the specifications laid down, same will be rectified within a shortest possible time. Thirty (30) days of free technical support through telephone/e-mail/chat (voice and non-voice) is included. Additional maintenance support options available on request.

Customization:

Best efforts have been made to ensure that the core has most relevant features and can fit into wide range of applications. However, the customer may require some specific functions in the core. The core can be customized or modified on customers request to meet their requirement specifications.

Target Technologies:

- **FPGA:** Spartan 3, Virtex, Virtex 2/Pro, Virtex 4, Virtex 5
- ASIC standard cell

Device utilization summary:

Target Device	Max. Frequency (MHz)	Slices used	Block RAMs
Spartan xc3s1500fg456	75	2181	4



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