



Overview:

The Direct Digital Synthesizer (DDS) is an IP core for digitally creating arbitrary waveforms and frequencies from a single, fixed source frequency. This DDS system takes a constant reference clock input and scales it down to a specified output frequency sampled at the reference clock frequency. This method of frequency control makes the IP core ideal for systems that require precise frequency sweeps like Radars.

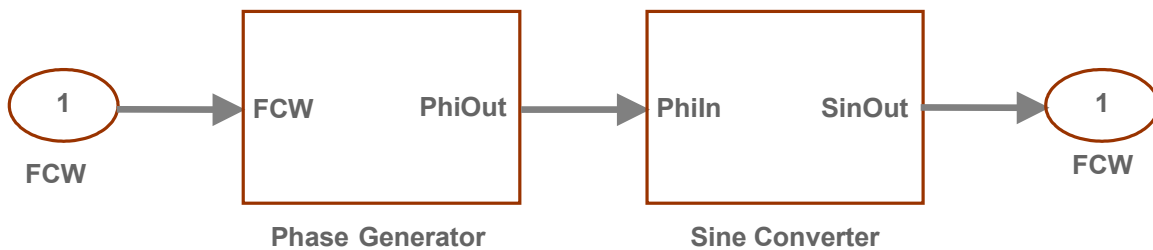
Features:

- Implemented using Piecewise Quadrature Sine Interpolation (PQSI) algorithm
- Sixteen segments per quadrate
- 1024 points per segment
- Very low memory requirements of 704 bits
- User selectable output resolution of 12 to 20 bits.
- Pipeline delay of 16/17 clocks for signed/unsigned output
- FCW (Frequency Control Word) resolution of 16 to 32 bits
- Low SFDR (Spurious Free Dynamic Range), better than 96 dB for output frequency range of 0.15 fclk to 0.20 fclk

Key Benefits:

- Low memory requirements
- High speed capabilities
- Technology independent IP core
- Highly optimized design with minimum usage of target device resources
- Parameterized HDL design
- FPGA proven for Xilinx Spartan-3 FPGA.
- Easily modifiable to meet specific client requirements
- RTL source code available for easy integration and implementation

Block diagram:

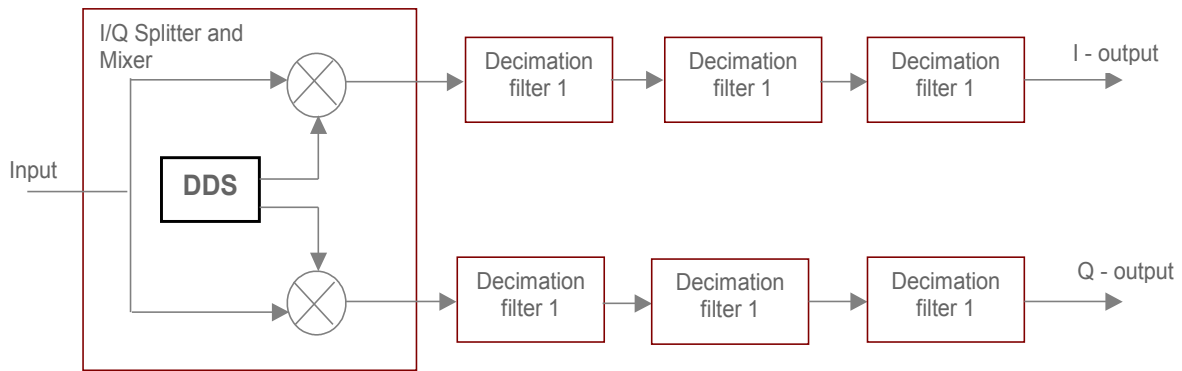


Applications:

- Digital radios and modems
- Software-Defined Radio's (SDR)
- Digital up/down converters for cellular and PCS base stations
- Waveform synthesis in Digital Phase Locked Loops
- Generating injection frequencies for analog mixers
- Demodulators/modulators.
- Tone generators

Application Note - Digital Down Converter (DDC):

DDC is composed of an I/Q splitter incorporating a DDS. DDC modulates the input signal coming from the RF section with sine and cosine waves by utilizing two mixers and a decimation section consisting of a series of FIR decimation filters.



Deliverables:

- Core options
 - RTL design in VHDL
 - Technology specific netlist
- Test bench
- Documentation

Support and warranty:

The core is code tested, extensively simulated and thoroughly verified on hardware board. The core is warranted against defects and meets the technical specifications. In rarest case, if the core has some defects or do not comply with the specifications laid down, same will be rectified within a shortest possible time. Thirty (30) days of free technical support through telephone/e-mail/chat (voice and non-voice) is included. Additional maintenance support options available on request.

Customization:

Best efforts have been made to ensure that the core has most relevant features and can fit into wide range of applications. However, the customer may require some specific functions in the core. The core can be customized or modified on customers request to meet their requirement specifications.

Target Technologies:

- **FPGA:** Spartan 3, Virtex, Virtex 2/Pro, Virtex 4, Virtex 5
- ASIC standard cell

Device utilization summary:

Target Device	Max. Frequency (in MHz)	No. of Slices used (out of 3584)	No. of 18x18 Multipliers (out of 16)
Xilinx Spartan XC3S400	131	334	3



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